Electronic Version
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[THIN FILM TRANSISTOR MANUFACTURE METHOD]

Abstract

A Thin Film Transistor (TFT) manufacture method, comprising manufacture of a gate, a gate isolation layer, a channel layer, and a source/drain. Wherein, the manufacture of the channel layer comprises: forming a first a-Si layer by using a low deposition rate (LDR) (Chemical Vapor Deposition, CVD); forming a second a-Si layer by using a high deposition rate (HDR); and forming an N+Mixed a-Si layer. When the first a-Si layer is formed in the present invention, the flux ratio of H_2/SiH_4 is adjusted to a range from 0.40 to 1.00 to increase the number of defects in the first a-Si layer. When the TFT is irradiated by the light, the photo leakage current generated in the channel layer is trapped in the defects in the first a-Si layer. Therefore, the TFT photo leakage current can be significantly reduced.